Please delete the text at page 5, lines 5 – 17 and enter the following as a clean version substitute for such paragraph:

An improved digital communications link of the present invention connects a digital controller section of an xDSL modem - which is preferably located on a system motherboard of a computing system - to a separate analog section of the xDSL modem - which is located at a position substantially free of electronic noise from other electronic components on said motherboard, which could materially affect the operation of such analog section. The data path/link is generally configured in the following manner: (a) a plurality of receive signal lines are set up for receiving data from a remote site; (b) a plurality of transmit signal lines are designated for transmitting data to a remote site; (c) a bit clock signal line is set up for carrying a clock signal, which clock signal is used in connection with communicating the data to and from the remote site. The bit clock signal line can carry any desired clock signal needed according to data transmission requirements of said digital communications link, thus providing a scalable interface that is easily adaptable for use in any number of different motherboard environments.

Please enter the following as a clean version substitute for the paragraph in the specification at page 10, lines 1 – 11:

216, which transmits signals in the DSL link to DSL Digital Modem Circuit 230, and converts received signals in the DSL link to various data and control signals for the internal circuits within DSL Analog Modem Circuit 205, including control registers 215. Also inside DSL-A 216 is a clock circuit (not shown) which generates the necessary clocks for internal blocks and external DSL link based on an input from a System Master Clock as shown. Again, some or all of the functions of DSL Analog Modem Circuit 205 may be grouped and implemented in single chip form. For example, DSL-A codec 218, incorporating control registers 215, DSL-A Interface 216, digital filters 214, 214', and A/D 213 and D/A 213' is preferably embodied in a single integrated circuit (IC), and a separate IC is preferably used to embody analog front end sections (i.e. receive/transmit drivers 209, 209' and receive/transmit filters 211 and 211').

Please enter the following as a clean version substitute for the paragraph in the specification at page 11, lines 27 – 29:

As noted above, functions performed by Transmitter Buffer and Processing 234' and Receiver Buffer and Processing 234 depend on the specific xDSL implementation. In the case of host signal processing, where the present invention can be used for great

Please enter the following as a clean version substitute for the paragraph in the specification at page 12, lines 24 – 26:

Receive data lines RX_1 - RX_4 carry digital samples generated by A/D 213 and assembled and transmitted across the link by DSL-A Interface 216; DSL-D interface 233, conversely dis-assembles and passes these samples on for further signal processing.

Please enter the following as a clean version substitute for the paragraph in the specification at page 18, lines 11 – 29:

--Reuse of DSL Link for External Hardware DSL Implementation

As mentioned earlier, the use of DSL Link 220 is most attractive to a host based DSL modem implementation requiring minimal logic inside Digital IC 230. When the CPU in the motherboard is not fast enough, it is desirable to use the DSL Link to connect Digital IC 230 to an external hardware DSL implementation. In this case, another useful aspect of the present invention is illustrated in FIG. 4. As shown, when an external hardware solution for a DSL modem implementation exists, a reasonable interface to use with such implementation is one based on the ATM Utopia I or Utopia II interface. This is because ADSL technology has already been defined to interface with ATM in both T1.413 Issue 2 and ITU-T G.992 standards. In this configuration, DSL Digital IC 230 would be linked through DSL Digital Link 220 to a hardware based xDSL modem in FIG. 2A and 2B, instead of interfacing directly to DSL Analog Modem Circuit 205. In such instance, of course, since most of the signal processing and control functions would be located within the hardware xDSL modem, DSL Digital Controller 230 could be simplified accordingly. The reason this is possible is because the same 10 signal lines described above (RX_1 - RX_4, TX_1 - TX_4, CLOCK and WORD CLOCK) can serve a dual purpose and act as an ATM interface as well. As above, for the same four sampling cycles per word clock, the following data can be transported over DSL digital link 220:

1. First clock cycle period: RX_1 - RX_4 are used for Control, 0, RxClav, TxClav;